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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/771,743	01/29/2001	Taku Yamagata	450100-02936	1150

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EXAMINER	
PATHAK, SUDHANSHU C	

ART UNIT	PAPER NUMBER
2634	4

DATE MAILED: 08/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/771,743	YAMAGATA ET AL.	
	Examiner	Art Unit	
	Sudhanshu C. Pathak	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *January 29th, 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3-6,9-12,15-18 and 21-24* is/are allowed.

6)☒ Claim(s) *1,2,7,8,13,14,19 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *January 29th, 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-to-24 are pending in the application.

Drawings

2. Figure 10 should be designated by a legend such as "Prior Art" because only that which is known is illustrated. Corrective Action is required.

Claim Objections

3. Claim19 objected to because of the following informalities:

Claim 19 refers to a "modulation method", this should actually be a "demodulation method". Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2 (apparatus) & 13-14 (method) are rejected under 35 U.S.C. 103(a) as being unpatentable over Akinori et al. (JP 10-229423 also referred to as Japanese Unexamined Patent Publication No. 09-28597 as disclosed in the Specification on Page 3, line 5) in view of Sato (5,343,502).

Regarding to Claims 1-2 & 13-14, Akinori discloses a timing error detection circuit and a demodulator for detecting a timing error of symbols arranged at a pre-determined symbol cycle included in a signal (Page 1 of 21,

Paragraph 1, Field of Invention & Page 7 of 21, Paragraph 39, Embodiment of the Invention, lines 1-5 & Drawing 1-2, element 7) comprising a sampling circuit for sampling said signal at a frequency equal to or more than double of a symbol rate (Page 1 of 21, Paragraph 2, lines 1-9 & Paragraph 3, lines 1-11 & Paragraph 4, lines 1-12 & Page 12 of 21, Paragraph 63, lines 1-9 & Drawings 1-2, 22, element 4). Akinori further discloses the received signal to include a phase shift modulated signal (Page 1 of 21, Paragraph 1, Field of Invention & Page 1 of 21, Paragraph 2, lines 1-9 & Paragraph 3, lines 1-11). However, Akinori does not disclose the timing error detection circuit to comprise an amplitude detection circuit for detecting amplitude at said sampled position; and a detection circuit for detecting the timing error based on difference of said detected plurality of amplitudes.

Sato discloses a symbol timing detection circuit for a receiver receiving a TDMA signal (Column 1, lines 5-10). The circuit comprising an amplitude detection circuit for detecting the amplitude at said sample position of the received signal (Fig. 1, element 1 & Column 1, lines 55-60 & Column 2, lines 63-68 & Column 3, lines 1-43); and a detection circuit for detecting the timing error based on the differences of said detected plurality of amplitudes (Fig. 1, element 3 & Fig. 3a-c & Abstract, lines 1-13 & Column 1, lines 43-68 & Column 2, lines 1-68 & Column 3, lines 1-43 & Claim 1). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Sato teaches determining the timing error based on the difference of the detected plurality of amplitudes and this can be implemented

in the timing error detection circuit and demodulator as described in Akinori replacing the phase detection circuit so as to provide accurate timing detection for a "bursty" received signal and further implementing the circuit in a compact LSI form wherein no circuit adjustments are required.

6. Claims 7-8 (apparatus), 19-20 (method) & 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view Akinori et al. (JP 10-229423 also referred to as Japanese Unexamined Patent Publication No. 09-28597 as disclosed in the Specification on Page 3, line 5) in further view of Sato (5,343,502) in further view of Yoshida (5,235,622).

Regarding to Claims 7-8 & 19-20, the AAPA discloses a demodulation circuit (Fig. 10 & Specification, Page 2, lines 7-8) comprising a symbol timing reproduction circuit for detecting the timing error of symbols and reproducing symbol timing based on the detected timing error (Fig. 10, element 101 & Specification, Page 2, lines 9-25 & Specification, Page 3, lines 1-4); a carrier reproduction circuit for performing carrier reproduction of the signal wherein said symbol timing is reproduced (Fig. 10, element 102 & Specification, Page 3, lines 1-18); a symbol decode circuit for decoding said symbol included in the carrier reproduced signal (Fig. 10, element 103 & Specification, Page 3, lines 19-23). However, the AAPA does not specify the symbol timing reproduction circuit to further comprise a sampling circuit for sampling the received signal at a frequency equal to or more than double the symbol rate or more.

Akinori discloses a timing error detection circuit and a demodulator for detecting a timing error of symbols arranged at a pre-determined symbol cycle included in a signal (Page 1 of 21, Paragraph 1, Field of Invention & Page 7 of 21, Paragraph 39, Embodiment of the Invention, lines 1-5 & Drawing 1-2, element 7) comprising a sampling circuit for sampling said signal at a frequency equal to or more than double of a symbol rate (Page 1 of 21, Paragraph 2, lines 1-9 & Paragraph 3, lines 1-11 & Paragraph 4, lines 1-12 & Page 12 of 21, Paragraph 63, lines 1-9 & Drawings 1-2, 22, element 4). Akinori further discloses the received signal to include a phase shift modulated signal (Page 1 of 21, Paragraph 1, Field of Invention & Page 1 of 21, Paragraph 2, lines 1-9 & Paragraph 3, lines 1-11). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Akinori teaches sampling the received signal at a frequency equal to two or more than the double of the symbol rate and this can be implemented in the demodulator circuit as described in the AAPA so as to accurately determine the timing reproduction from the received data. However, AAPA in view of Akinori does not disclose the timing error detection circuit to comprise an amplitude detection circuit for detecting amplitude at said sampled position; and a detection circuit for detecting the timing error based on difference of said detected plurality of amplitudes.

Sato discloses a symbol timing detection circuit for a receiver receiving a TDMA signal (Column 1, lines 5-10). The circuit comprising an amplitude detection circuit for detecting the amplitude at said sample position of the

received signal (Fig. 1, element 1 & Column 1, lines 55-60 & Column 2, lines 63-68 & Column 3, lines 1-43); and a detection circuit for detecting the timing error based on the differences of said detected plurality of amplitudes (Fig. 1, element 3 & Fig. 3a-c & Abstract, lines 1-13 & Column 1, lines 43-68 & Column 2, lines 1-68 & Column 3, lines 1-43 & Claim 1). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Sato teaches determining the timing error based on the difference of the detected plurality of amplitudes and this can be implemented in the timing error detection circuit and demodulator as described in AAPA in view of Akinori replacing the phase detection circuit so as to provide accurate timing detection for a "bursty" received signal and further implementing the circuit in a compact LSI form wherein no circuit adjustments are required. However, AAPA in view of Akinori in further view of Sato does not disclose an interpolator circuit for reproducing the symbol timing by performing interpolation processing on the received signal based on the detected timing error.

Yoshida discloses an clock recovery circuit for demodulation of a received APSK signal (Abstract, lines 1-24) comprising an interpolator circuit for reproducing the symbol timing by performing interpolation processing on the received signal based on the detected timing error (Fig. 2, element 14 & Column 2, lines 13-20 & Column 4, lines 23-40). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Yoshida teaches implementing an interpolator for reproducing the symbol

timing by performing interpolation processing on the received signal based on the detected timing error and this can be implemented in the demodulator circuit as described in AAPA in view of Akinori in further view of Sato so as to provide a more accurate (more samples) received signal for further demodulation and decoding and also minimize the complexity of the sampling (ADC) in the earlier receiving chain.

Allowable Subject Matter

7. Claims 3-6, 9-12, 15-18 & 21-24 are allowable over the prior art of record because the cited references do not contain the specified limitation of an demodulator circuit comprising a timing error detection circuit for detecting the timing error of symbols arranged at a pre determined symbol cycle comprising an interpolator circuit for generating data at time "T/4" using the sampled data at time "0" and "T/2" and generating data at time "3T/4" using the sampled data at time "T/2" and "T" when assuming a symbol appears at times "0" and "T"; an amplitude detection circuit for detecting an amplitude of the signal at the position from data at said time "T/4" and time "3T/4"; and a detection circuit for detecting the direction and amount of said timing error based on the large or small relationship of the difference of the amplitude at said time "T/4" and the amplitude at said time "3T/4".

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sudhanshu C. Pathak whose

telephone number is (703)-305-0341. The examiner can normally be reached on M-F: 9am-6pm.

- If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (703)-305-4714.
- The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.
- Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sudhanshu C. Pathak

STEPHEN CHIN
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